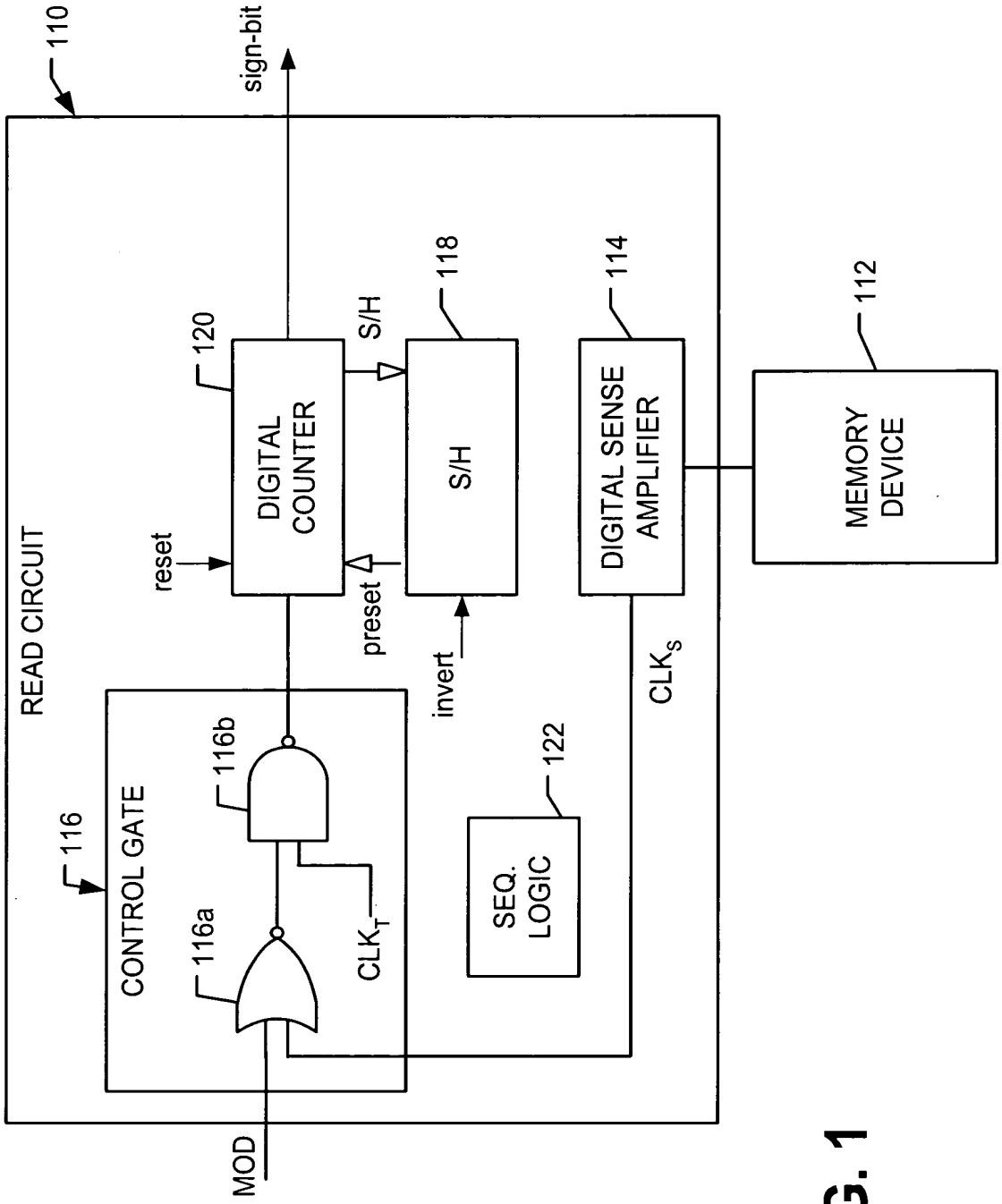

110
sign-bit
READ CIRCUIT
120
DIGITAL COUNTER
S/H
118
S/H
114
DIGITAL SENSE AMPLIFIER
112
MEMORY DEVICE
reset
preset
invert
CLK_S
116
CONTROL GATE
116b
116a
CLK_T
122
SEQ. LOGIC
MOD

FIG. 1

FIG. 3a

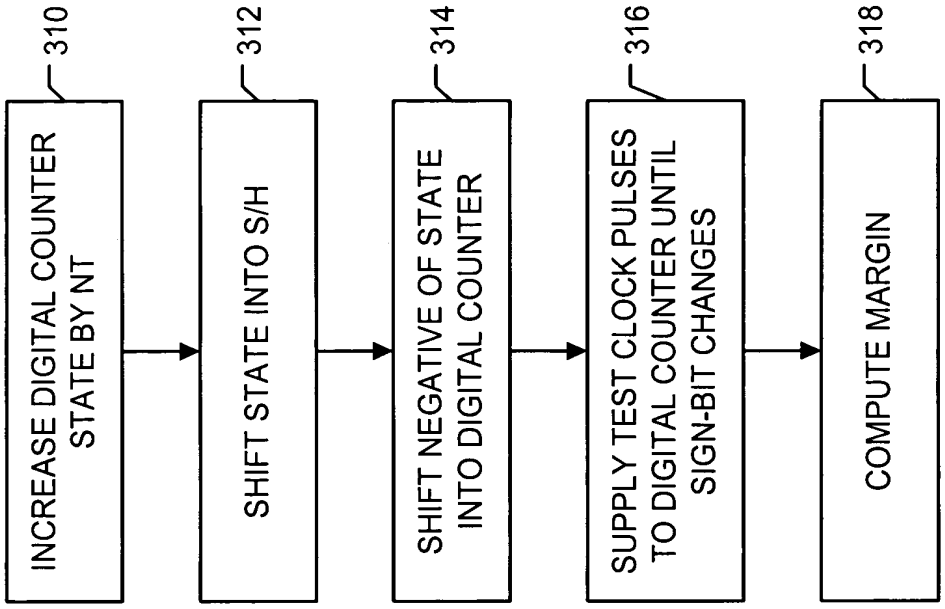

310
INCREASE DIGITAL COUNTER STATE BY NT
312
SHIFT STATE INTO S/H
314
SHIFT NEGATIVE OF STATE INTO DIGITAL COUNTER
316
SUPPLY TEST CLOCK PULSES TO DIGITAL COUNTER UNTIL SIGN-BIT CHANGES
318
COMPUTE MARGIN

FIG. 2

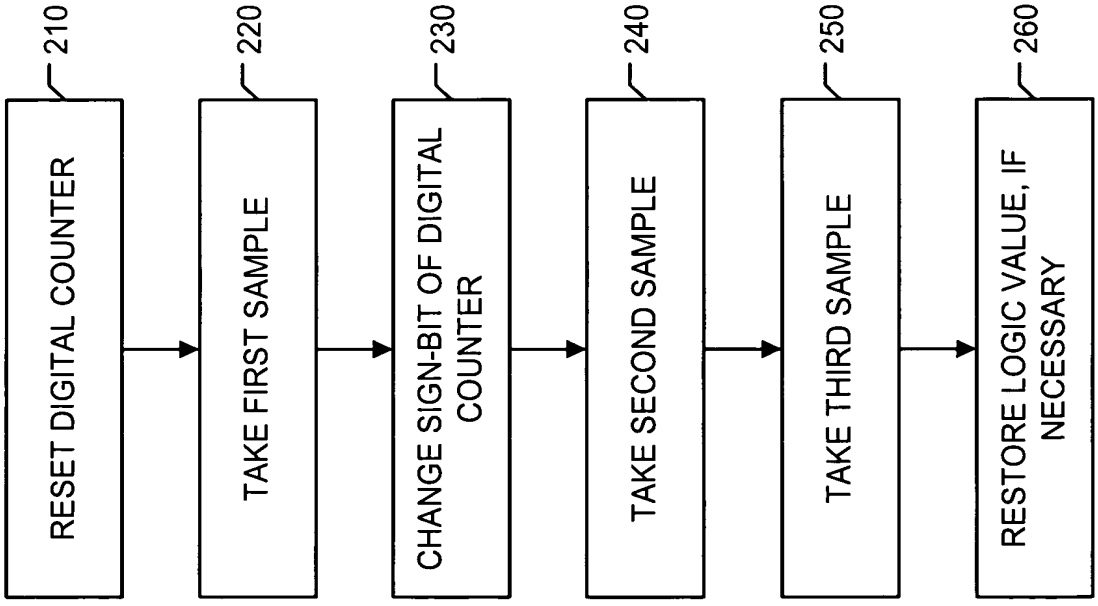

210
RESET DIGITAL COUNTER
220
TAKE FIRST SAMPLE
230
CHANGE SIGN-BIT OF DIGITAL COUNTER
240
TAKE SECOND SAMPLE
250
TAKE THIRD SAMPLE
260
RESTORE LOGIC VALUE, IF NECESSARY

FIG. 3C

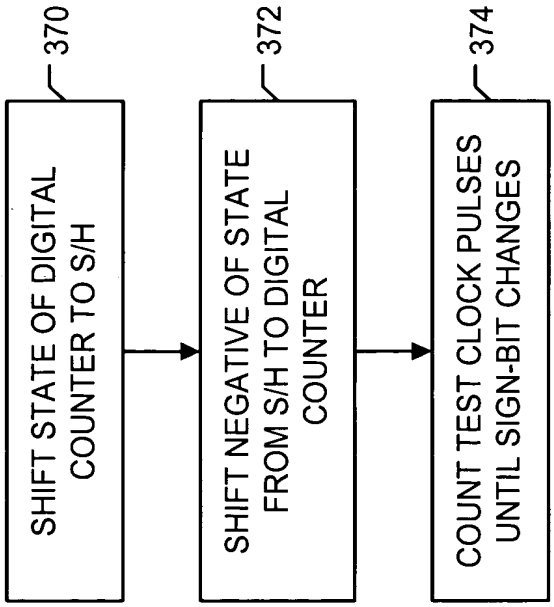
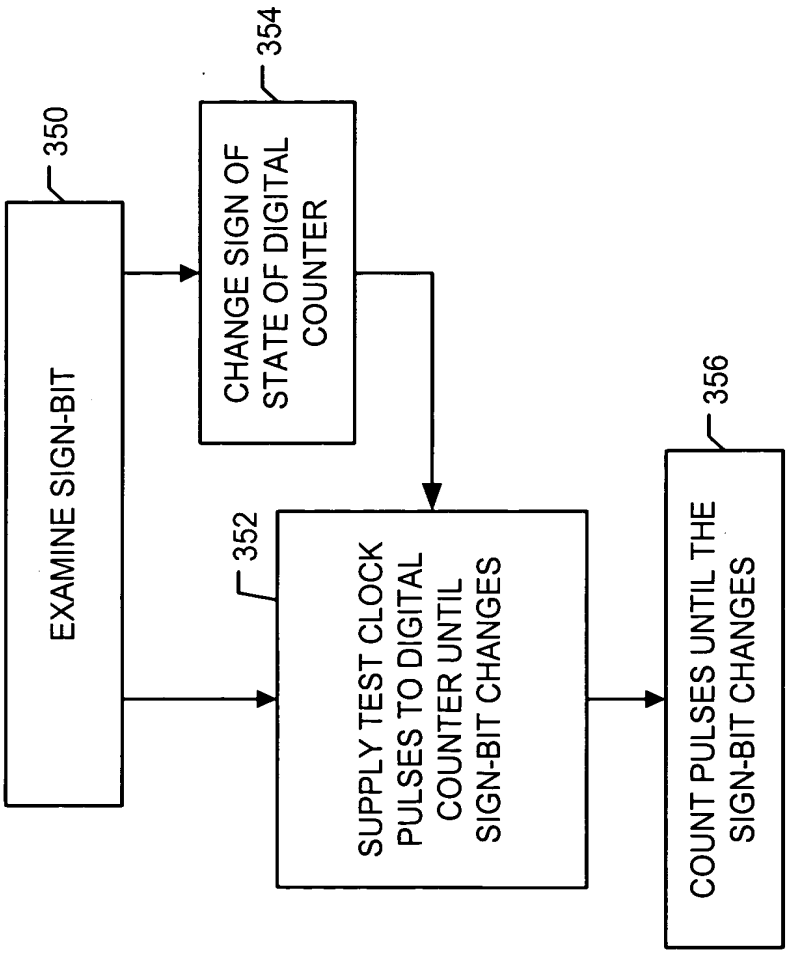

370
SHIFT STATE OF DIGITAL COUNTER TO S/H
372
SHIFT NEGATIVE OF STATE FROM S/H TO DIGITAL COUNTER
374
COUNT TEST CLOCK PULSES UNTIL SIGN-BIT CHANGES

FIG. 3b


350
EXAMINE SIGN-BIT
354
CHANGE SIGN OF STATE OF DIGITAL COUNTER
352
SUPPLY TEST CLOCK PULSES TO DIGITAL COUNTER UNTIL SIGN-BIT CHANGES
356
COUNT PULSES UNTIL THE SIGN-BIT CHANGES

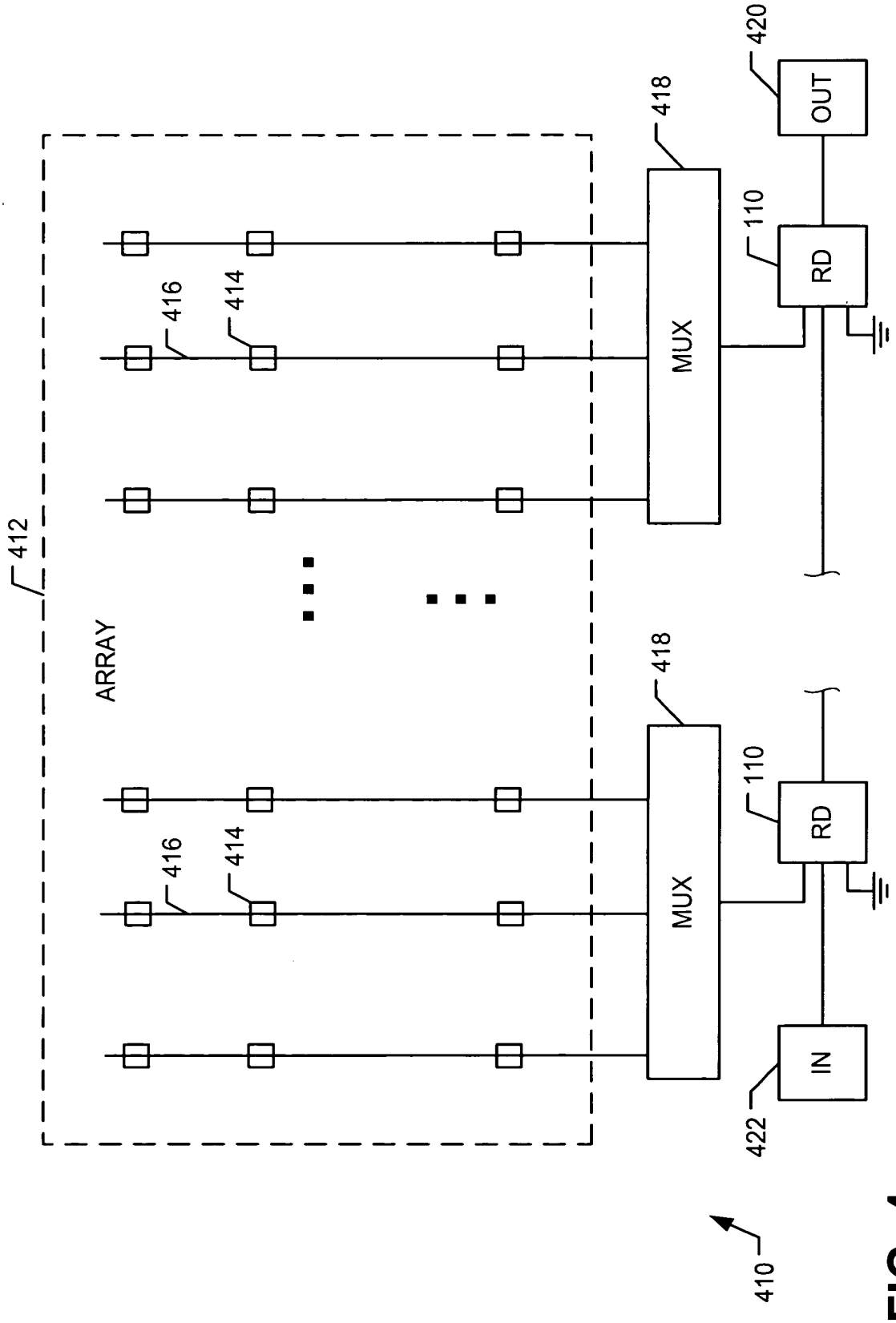
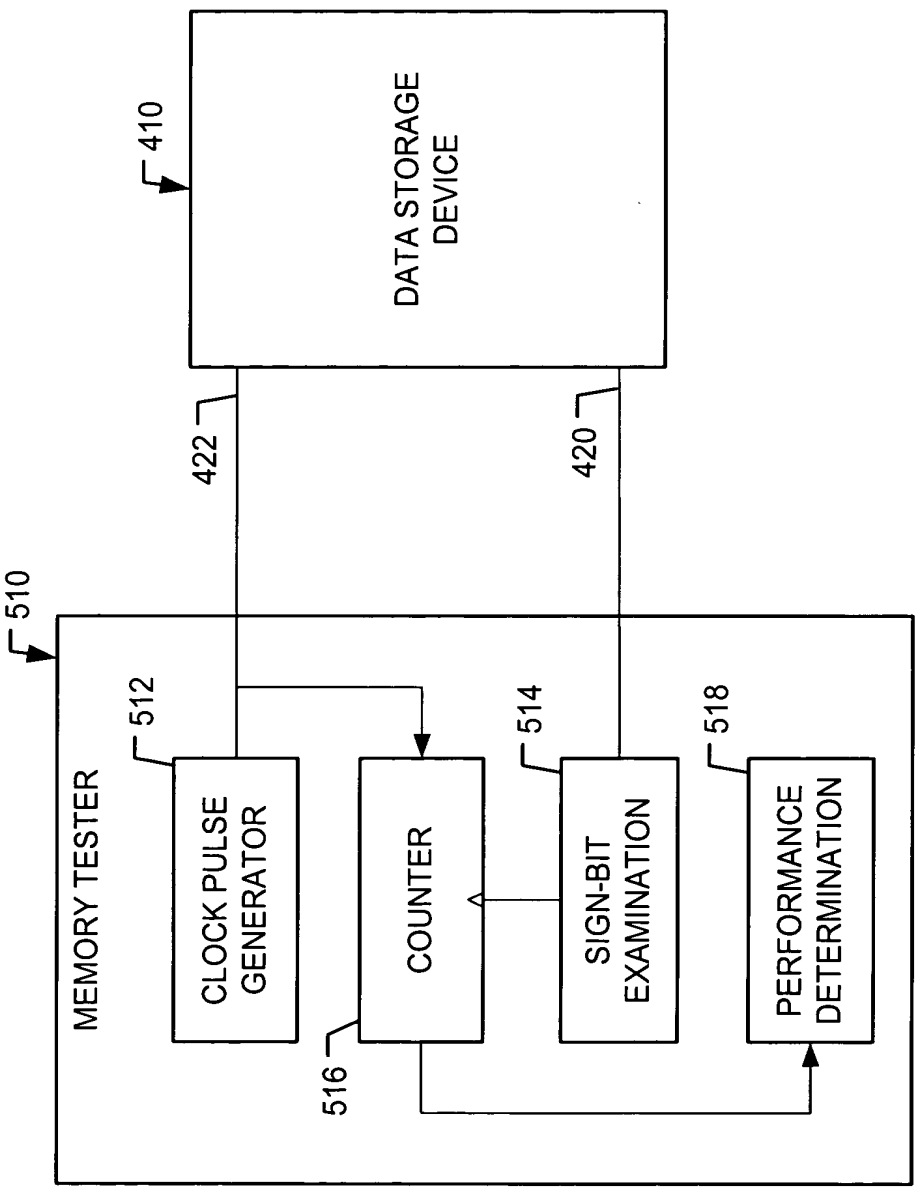


FIG. 4

FIG. 5


410
DATA STORAGE DEVICE
422
420
510
MEMORY TESTER
512
CLOCK PULSE GENERATOR
COUNTER
514
SIGN-BIT EXAMINATION
518
PERFORMANCE DETERMINATION
516